CNC3X Series

High Capacitance Stacked Capacitors

ESA Qualified

FEATURES

- Multilayer chips ceramic capacitors stacked
- X7R dielectric (NP0 available on request)
- Capacitance range: 1.2µF to 68µF
- Voltage range: 16 V_{DC} to 25 V_{DC}
- Their low operating voltage give them a major advantage as they have much higher capacitance values in the same format. These components are ideally suited to advanced digital electronic applications requiring ever lower operating voltages

PHYSICAL CHARACTERISTICS

CONSTRUCTION

- P, PL, L models: DIL leaded uncoated stacked chips capacitors for surface mounting recommended to eliminate thermomechanical stresses.
- N, NU models: DIL leaded stacked chips capacitors for through-hole circuits (N: varnished, NU: uncoated chips)
- They can be supplied on request in ribbon or molded configuration

MARKING (clear or coded)

Capacitance value, tolerance, rated voltage (except 16 V).

ELECTRICAL SPECIFICATIONS

DIELECTRIC	X7R
Maximum ΔC/°C over temperature range without voltage	±15%
Ageing	≤ 2.5% per decade hour
Operating temperature	−55°C +125°C
Rated voltage (U_{RC})	16 V_{DC} to 25 V_{DC}
Dielectric withstanding voltage	2.5 U_{RC}
Capacitance	at 1kHz 0.3Vrms
Dissipation factor	≤2.5% at 1kHz 0.3Vrms
Insulation resistance at 25°C under U_{RC}	≥ 1,000 MΩ.µF

HOW TO ORDER

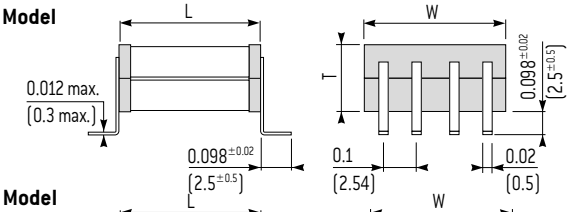
CNC	33	P	W	F	6,8µF	±10%	25 V
Series	Exxelia size code	Model	RoHS Compliant	Quality level	Capacitance	Tolerance	Rated voltage
CNC	**31** **32** **33** **34**	**P** **PL** **L** **N** **NU**	**-** = No RoHS **W** = RoHS compliant	**-** = standard quality level **F** = Hi-Rel quality: screening in accordance with Exxelia specification	Capacitance value in clear	**±10%** **±20%**	**16 V** **25 V**

High Capacitance Stacked Capacitors

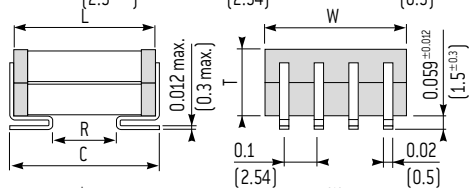
CNC3X Series

DIMENSIONS in inches (mm)

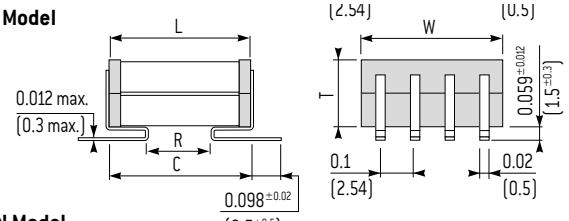
L Model



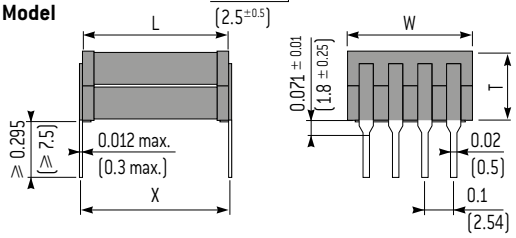
P Model



PL Model



N Model



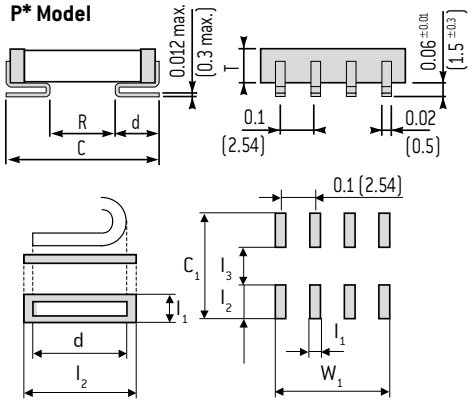
STANDARD RATINGS

Size	Series	Dimensions inches (mm)					Leads per side	T max.		Nb. of chips	Rated Voltage		Min. cap. Value
		L max.	W max.	R min.	C max.	X		inches	(mm)		16 V	25 V	
2220	CNC31	0.296 (7.5)	0.237 (6)	0.098 (2.5)	0.296 (7.5)	0.2 ± 0.020 (5.08 ± 0.5)	2	0.099 0.197 0.296	(2.5) (5) (7.5)	1 2 3	3.9µF 6.8µF 12µF	2.2µF 4.7µF 6.8µF	1.2µF
2528	CNC32	0.315 (8)	0.315 (8)	0.098 (2.5)	0.315 (8)	0.3 ± 0.020 (7.62 ± 0.5)	3	0.099 0.197 0.296	(2.5) (5) (7.5)	1 2 3	4.7µF 10µF 15µF	3.3µF 5.6µF 10µF	1.8µF
3333	CNC33	0.394 (10)	0.363 (9.2)	0.137 (3.5)	0.394 (10)	0.3 ± 0.020 (7.62 ± 0.5)	3	0.099 0.197 0.296 0.394	(2.5) (5) (7.5) (10)	1 2 3 4	8.2µF 15µF 22µF 33µF	5.6µF 10µF 15µF 22µF	3.3µF
4040	CNC34	0.493 (12.5)	0.473 (12)	0.196 (5)	0.493 (12.5)	0.4 ± 0.020 (10.16 ± 0.5)	4	0.099 0.197 0.296 0.394	(2.5) (5) (7.5) (10)	1 2 3 4	15µF 27µF 47µF 68µF	10µF 18µF 27µF 39µF	5.6µF

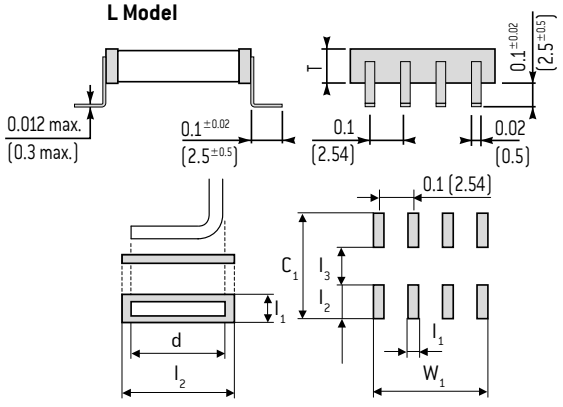
Available capacitance values: E6, E12 (see page XX). Specific values upon request.
The above table defines the standard products, other components may be built upon request.

RECOMMENDED FOOTPRINT

P* Model



L Model



Exxelia size code	Lead shape	C max inches (mm)		Leads per side	d inches (mm)		C_1 inches (mm)		W_1 inches (mm)		l_1 inches (mm)		l_2 inches (mm)		l_3 inches (mm)	
31	P*	0.295	(7.5)	2	0.059 ±0.012	(1.5 ±0.3)	0.335	(8.5)	0.147	(3.74)	0.047	(1.2)	0.128	(3.25)	0.079	(2)
	L	0.512	(13)	2	0.098 ±0.02	(2.5 ±0.5)	0.551	(14)	0.147	(3.74)	0.047	(1.2)	0.187	(4.75)	0.177	(4.5)
32	P*	0.315	(8)	3	0.087 ±0.012	(2.2 ±0.3)	0.354	(9)	0.247	(6.28)	0.047	(1.2)	0.138	(3.5)	0.079	(2)
	L	0.531	(13.5)	3	0.098 ±0.02	(2.5 ±0.5)	0.571	(14.5)	0.247	(6.28)	0.047	(1.2)	0.187	(4.75)	0.197	(5)
33	P*	0.394	(10)	3	0.087 ±0.012	(2.2 ±0.3)	0.433	(11)	0.247	(6.28)	0.047	(1.2)	0.157	(4)	0.118	(3)
	L	0.610	(15.5)	3	0.098 ±0.02	(2.5 ±0.5)	0.650	(16.5)	0.247	(6.28)	0.047	(1.2)	0.187	(4.75)	0.276	(7)
34	P*	0.492	(12.5)	4	0.087 ±0.012	(2.2 ±0.3)	0.531	(13.5)	0.347	(8.82)	0.047	(1.2)	0.177	(4.5)	0.177	(4.5)
	L	0.709	(18)	4	0.098 ±0.02	(2.5 ±0.5)	0.748	(19)	0.347	(8.82)	0.047	(1.2)	0.187	(4.75)	0.374	(9.5)

* For PL : add 0.098 in (2.5 mm) to d and l2 and 0.197 in (5 mm) to C1.

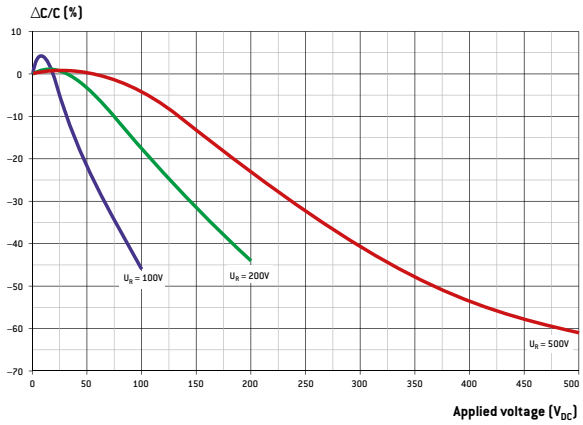
General Information

These capacitors have been developed in response to demand from switched mode power supply (S.M.P.S.) and DC-DC converters manufacturers. They are particularly suitable for filtering, smoothing and decoupling purpose in Hi-Rel equipments. The capacitors utilize advanced ceramic technology to achieve Hi-Rel long operating life and small size. They are designed for hybrid assemblies and low profile printed circuit applications.

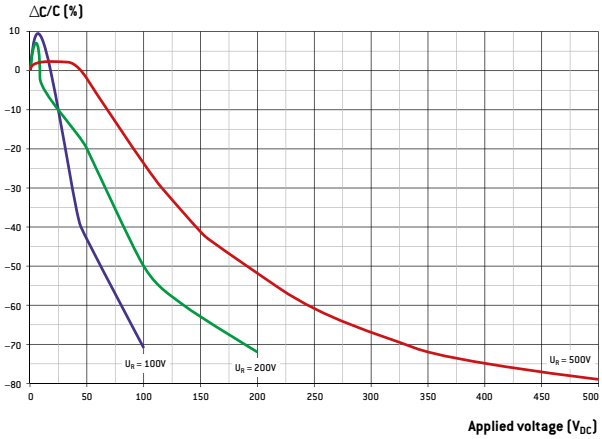
Customized assemblies may be achieved with standard bare chip sizes mentioned in the following chapters.

TYPICAL CURVES: R Series, SC/SV Series

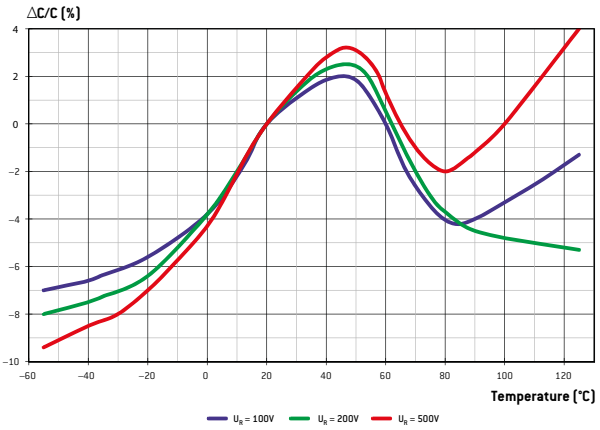
X DIELECTRIC: TYPICAL VOLTAGE COEFFICIENT AT 25°C (FOR ALL SIZES)



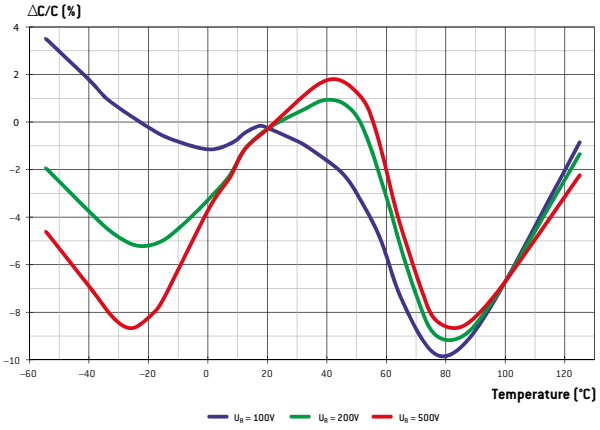
T DIELECTRIC: TYPICAL VOLTAGE COEFFICIENT AT 25°C (for all sizes)



X DIELECTRIC: TYPICAL TEMPERATURE COEFFICIENT WITHOUT VOLTAGE (for all sizes)

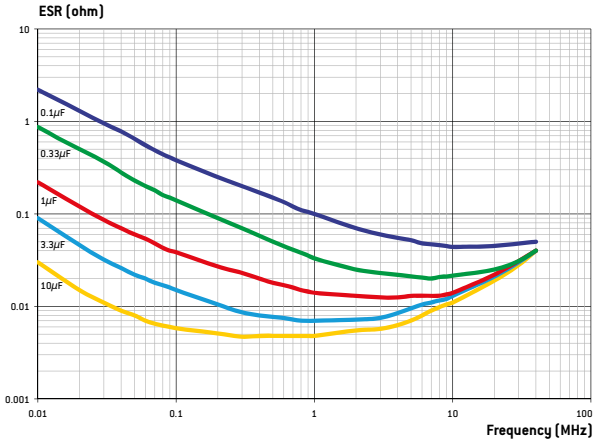


T DIELECTRIC: TYPICAL TEMPERATURE COEFFICIENT WITHOUT VOLTAGE (for all sizes)



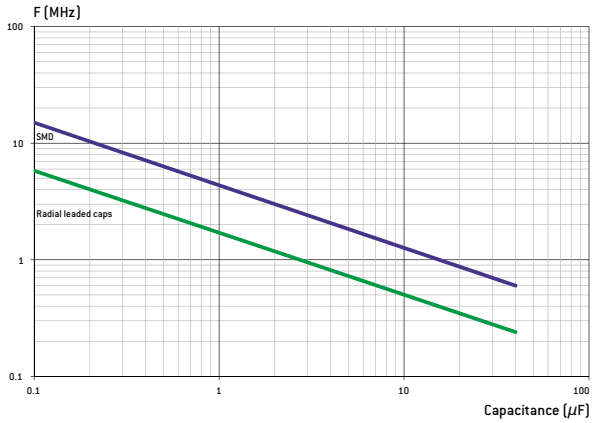
TYPICAL CURVES: R Series, SC/SV Series

TYPICAL ESR VS FREQUENCY

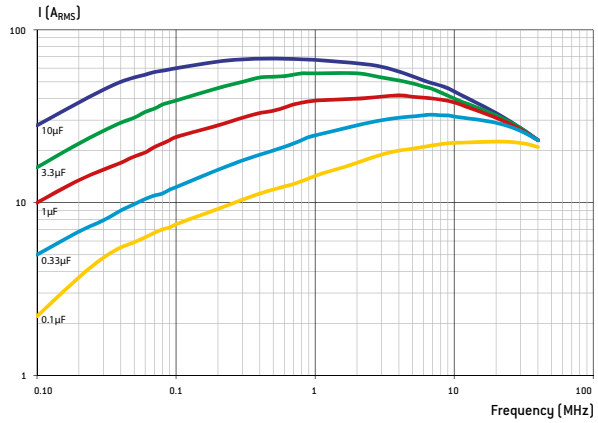


The ESR (Equivalent Serial Resistance) curves are given here for SMD (chips all case sizes) capacitors. Regarding the curves for the leaded capacitors, they are rather the same. ndeed, due to the resistivity of the raw material used and the wire diameters, the resistance of the wires is much lower than the ESR of the chips. So, in a first approach, their influence can be considered as negligible.

TYPICAL ESR VS FREQUENCY



TYPICAL MAXIMUM ADMISSIBLE CURRENT VS FREQUENCY

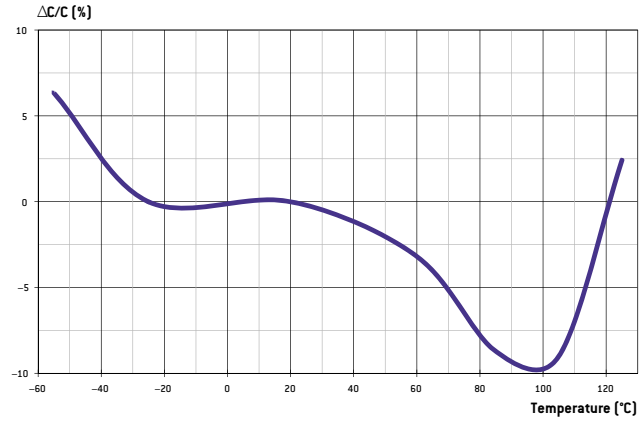


These typical curves are an example of admissible currents for one family of chip capacitors: 501R3740X chip series. For other curves and products or for further information, please contact us. Note: for the calculations, we have considered that the terminations are directly connected to an infinite heat sink. In other words, the thermal resistance of the circuit itself which depends of its type and design has not been taken into account. Moreover, the ambient temperature taken is 25°C.

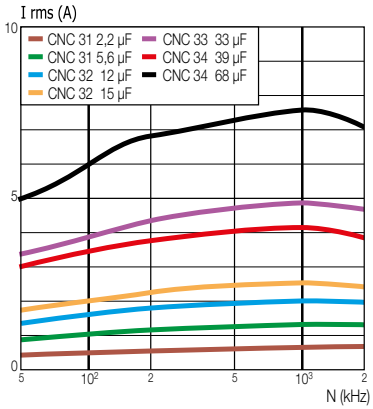
General Information

TYPICAL CURVES: CNC3X Series

TYPICAL TEMPERATURE COEFFICIENT

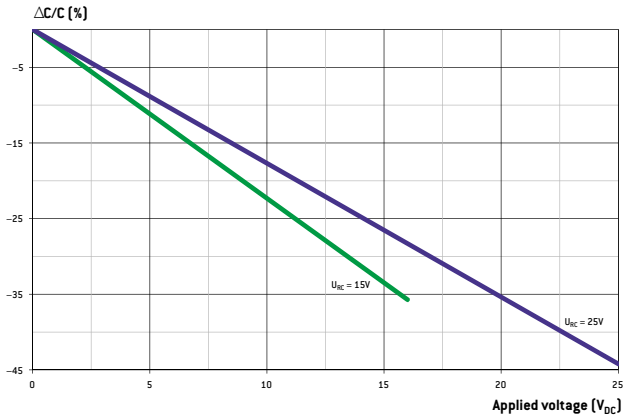


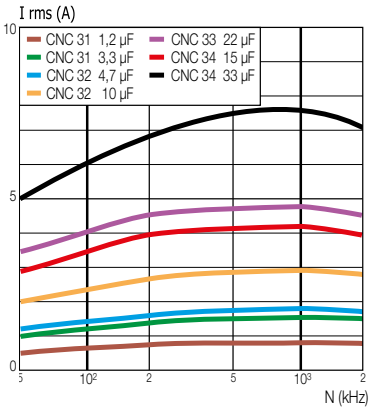
MAXIMUM CURRENT VS FREQUENCY



U_{RC} = 16V $_{DC}$ (Typical curves for Δθ = 20°C).

TYPICAL VOLTAGE COEFFICIENT

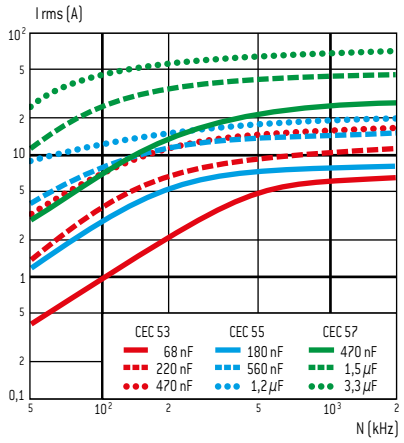




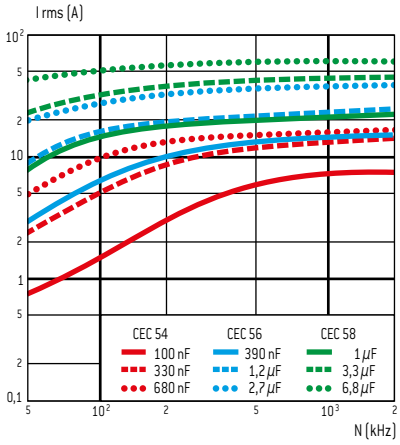
U_{RC} = 25 V $_{DC}$ (Typical curves for Δθ = 20°C).

TYPICAL CURVES: CEC5X Series

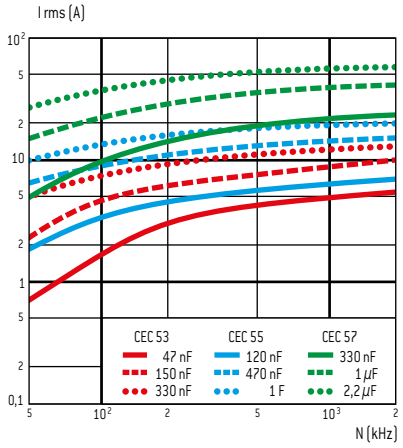
NPO: CURRENT VS FREQUENCY



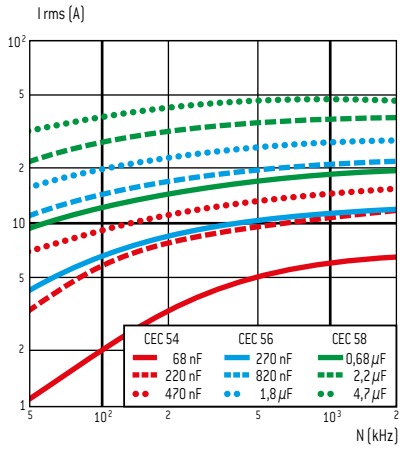
$U_{RC} = 63\ V_{DC}$ (Typical curve for $\Delta\theta = 20°C$).



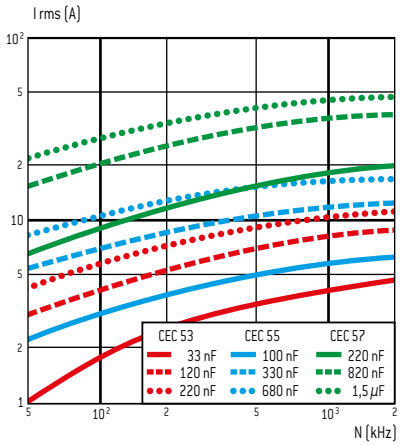
$U_{RC} = 63\ V_{DC}$ (Typical curve for $\Delta\theta = 20°C$).



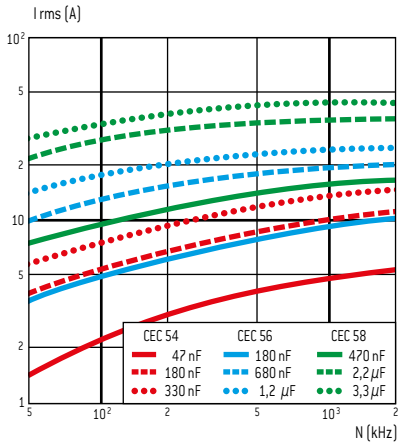
$U_{RC} = 100\ V_{DC}$ (Typical curve for $\Delta\theta = 20°C$).



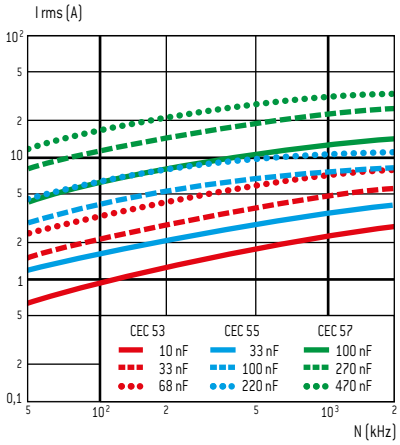
$U_{RC} = 100\ V_{DC}$ (Typical curve for $\Delta\theta = 20°C$).



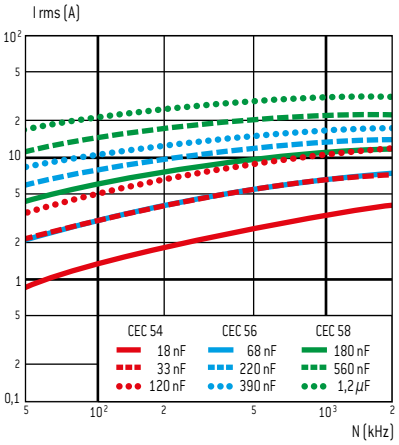
$U_{RC} = 200\ V_{DC}$ (Typical curve for $\Delta\theta = 20°C$).



$U_{RC} = 200\ V_{DC}$ (Typical curve for $\Delta\theta = 20°C$).



$U_{RC} = 500\ V_{DC}$ (Typical curve for $\Delta\theta = 20°C$).

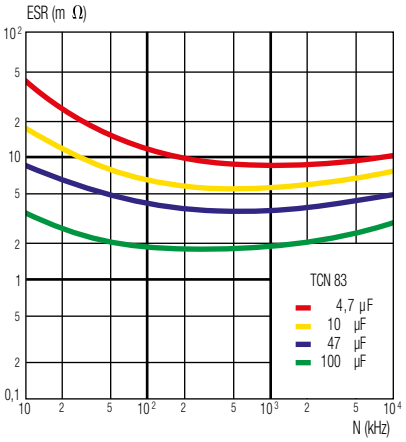


$U_{RC} = 500\ V_{DC}$ (Typical curve for $\Delta\theta = 20°C$).

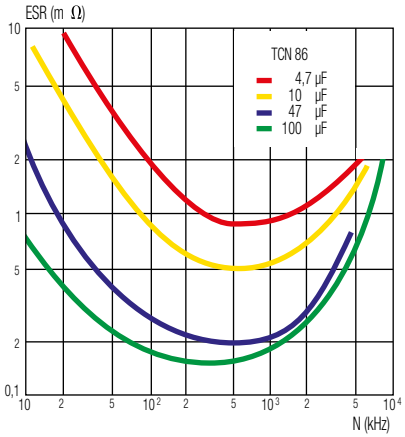
General Information

TYPICAL CURVES: TCN8X Series

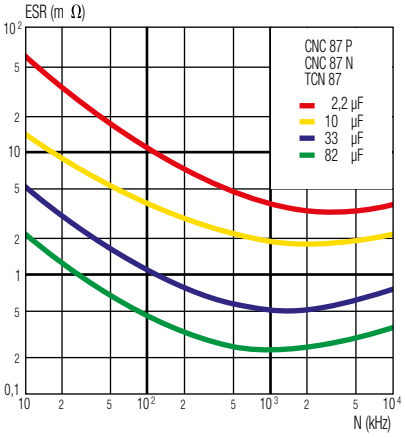
TCN83: TYPICAL EQUIVALENT SERIAL RESISTANCE (ESR) VS FREQUENCY (N)



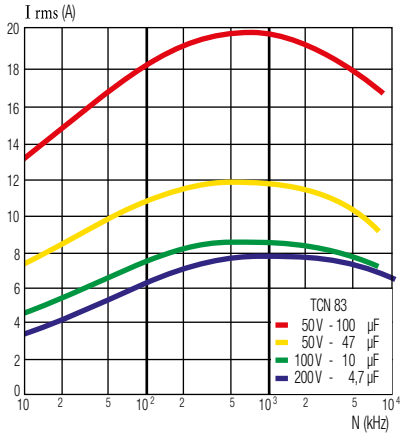
TCN86: TYPICAL EQUIVALENT SERIAL RESISTANCE (ESR) VS FREQUENCY (N)



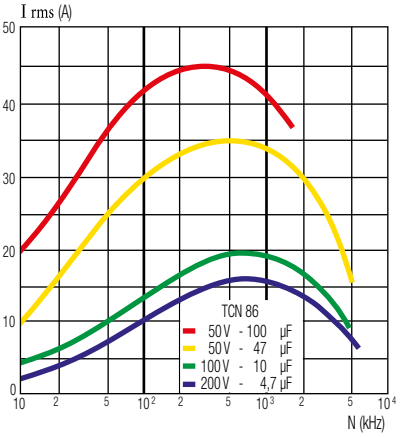
TCN87: TYPICAL EQUIVALENT SERIAL RESISTANCE (ESR) VS FREQUENCY (N)



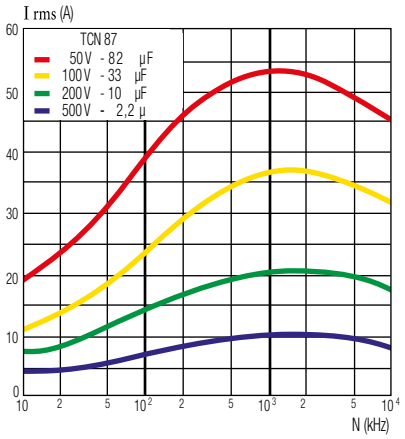
TCN83: CURRENT (I_{RMS}) VS FREQUENCY (N) TYPICAL CURVES FOR $\Delta\Theta \leq 20°C$



TCN86: CURRENT (I_{RMS}) VS FREQUENCY (N) TYPICAL CURVES FOR $\Delta\Theta \leq 20°C$

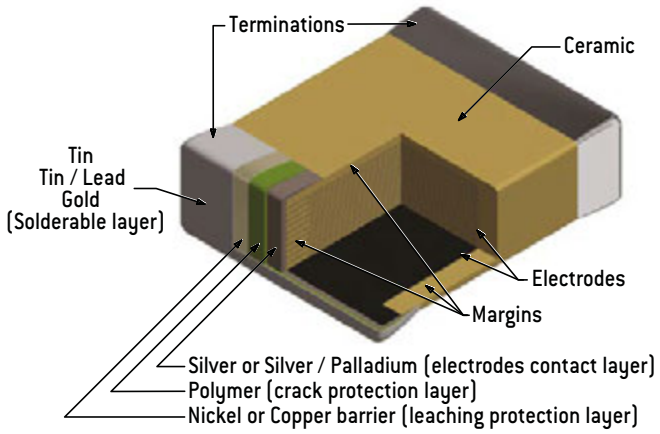


TCN87: CURRENT (I_{RMS}) VS FREQUENCY (N) TYPICAL CURVES FOR $\Delta\Theta \leq 20°C$



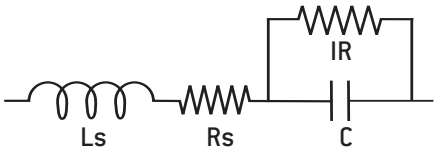
Ceramic Capacitors Technology

MLCC STRUCTURE



EQUIVALENT CIRCUIT

Capacitor is a complex component combining resistive, inductive and capacitive phenomena. A simplified schematic for the equivalent circuit is:



DIELECTRIC CHARACTERISTICS

Insulation Resistance (IR) is the resistance measured under DC voltage across the terminals of the capacitor and consists principally of the parallel resistance shown in the equivalent circuit. As capacitance values and hence the area of dielectric increases, the IR decreases and hence the product (C x IR) is often specified in Ω.F or MΩ.μF.

The Equivalent Series Resistance (ESR) is the sum of the resistive terms which generate heating when capacitor is used under AC voltage at a given frequency (f).

Dissipation factor (DF) is the ration of the apparent power input will turn to heat in the capacitor:

$DF = 2\pi f C ESR$

When a capacitor works under AC voltage, **heat power loss (P),** expressed in Watt, is equal to:

$P = 2\pi f C Vrms^2 DF$

The series inductance (Ls) is due to the currents running through the electrodes. It can distort the operation of the capacitor at high frequency where the **impedance (Z)** is given as:

$Z = Rs + j (Ls.\omega - 1/(C.\omega))$ with $\omega = 2\pi f$

When frequency rises, the capacitive component of capacitors is gradually canceled up to the resonance frequency, where :

$Z = Rs$ and $LsC.\omega^2 = 1$

Above this frequency the capacitor behaves like an inductor.

	P100	NP0	N2200 (C4xx)	BX	2C1	X7R
Dielectric material	Porcelain	Magnesium titanate or Neodynium baryum titanate	Barium zirconate titanate	Baryum titanate ($BaTiO_3$)		
Dielectric constant	15 – 18	20 – 85	450	2,000 – 5,000		
Electrode technology	PME (Precious Metal Electrodes): Ag/Pd					
Capacitance variation between –-55°C and +125/° C without DC voltage	(100±30)ppm/° C	(0±30)ppm/° C	(–2,200±500) ppm/° C	±15%	±20%	±15%
Capacitance variation between –-55°C and +125/° C with DC rated voltage			0 -15%	15% –25%	20% –30%	Not applicable
Piezo-electric effect	None		None	Yes		
Dielectric absorption	None		Few %	Few %		
Thermal shock sensitive	+		+	++		

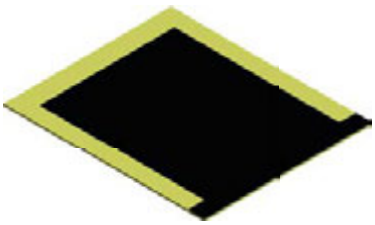
Ceramic Capacitors Technology

MANUFACTURING STEPS

SLIP CASTING

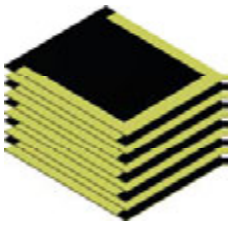
A slurry, a mix of ceramic powder, binder and solvents, is poured onto conveyor belt inside a drying oven, resulting in a dry ceramic sheet.

ELECTRODE SCREEN PRINTING



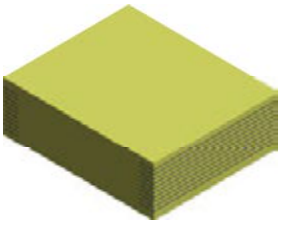
The electrode ink, made from a metal powder mixed with solvents, is printed onto the ceramic sheets using a screen printing process.

STACKING



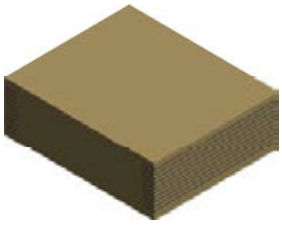
The sheets with electrode printed are stacked to create a multilayer structure.

PRESSING



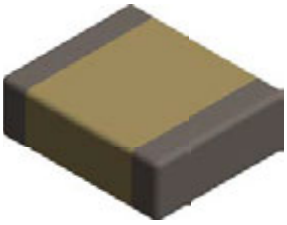
Pressure is applied to the stack to fuse all the separate layers, this created a monolithic structure.

SINTERING



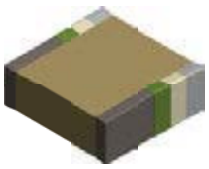
The parts are sintered in an oven with a precise temperature profile which is very important to the characteristics of the capacitors.

TERMINATIONS



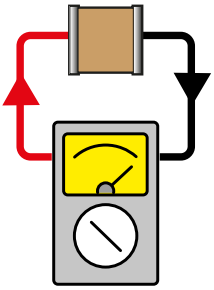
Each terminal of the capacitor is dipped in the termination ink, mix of metal powder, solvents and glass frit and the parts are fired in an oven.

TERMINATIONS PLATING



Stacking + leads soldering + encapsulation
(see pages 10-11)

FINAL TESTING



PACKAGING

User Guide

SMD TERMINATIONS

NON RoHS COMPLIANT	Code	RoHS COMPLIANT	Code	Magnetic	Recommended mounting process						Storage (months)*
					Epoxy bonding	Iron soldering	Wave soldering	Vapor phase soldering	Infrared soldering	Wire bonding	
Ag	**Q**	Ag	**QW / P**	No	●	●	●	●			18
Ag/Pd/Pt	**-**	Ag/Pd/Pt	**W / A**	No	●	●	●				24
Ag + Ni + dipped Sn/Pb 60/40	**T****	-	**-**	No		●	●	●	●		24
Ag/Pd/Pt + dipped Sn/Pb 60/40	**H**	Ag/Pd/Pt + dipped Sn	**HW**	No		●					24
Ag + Ni + electrolytic Sn/Pb 95/5	**C**	Ag + Ni + electrolytic Sn	**CW / S**	Yes		●	●	●	●		18
Ag + Ni + electrolytic Sn/Pb 60/40	**D**	-	**-**	Yes		●	●	●	●		18
-	**-**	Ag + Cu + electrolytic Sn	**C*****	No		●	●	●	●		18
Ag + Ni + dipped Sn/Pb 60/40	**E**	Ag + Ni + electrolytic Sn	**EW**	Yes		●	●				24
Ag + Ni + Au	**G**	Ag + Ni + Au	**GW**	Yes	●	●	●	●	●	●	36
Ag + Polymer + Ni + Sn/Pb 95/5	**YC**	Ag + Polymer + Ni + Sn	**YCW**	Yes		●	●	●	●		18
Ag + Polymer + Ni + Sn/Pb 60/40	**YD**	-	**-**	Yes		●	●	●	●		18
Ag + Polymer + Ni + Au	**YG**	Ag + Polymer + Ni + Au	**YGW**	Yes	●	●	●	●	●	●	36

Nickel (Ni) or Copper (Cu) barriers amplify thermal shock and are not recommended for chip sizes larger than 3030.

* Storage must be in a dry environment at a temperature of 20° C with a relative humidity below 50%, or preferably in a package enclosing a desiccant.
** Maintenance only.
*** Non magnetic chips series only.

SMD ENVIRONMENTAL TESTS

Ceramic chip capacitors for SMD are designed to meet test requirements of **CECC 32100** and **NF C 93133** standards as specified below in compliance with NF C 20700 and IEC 68 standards:

- Solderability: **NF C 20758,** 260° C, bath 62/36/2.
- Adherence: 5N force.
- Vibration fatigue test: **NF C 20706,** 20 g, 10 Hz to 2,000 Hz, 12 cycles of 20 minutes each.
- Rapid temperature change: **NF C 20714,** – –55°C to + 125° C, 5 cycles.
- Combined climatic test: **IEC 68-2-38.**
- Damp heat: **NF C 20703,** 93 %, H.R., 40° C.
- Endurance test: 1,000 hours, 1.5 U_{RC}, 125° C.

STORAGE OF CHIP CAPACITORS

TINNED OR NON TINNED CHIP CAPACITORS

Storage must be in a dry environment at a temperature of 20°C with a relative humidity below 50 %, or preferably in a packaging enclosing a desiccant.

STORAGE IN INDUSTRIAL ENVIRONMENT:

- 2 years for tin dipped chip capacitors,
- 18 months for tin electroplated chip capacitors,
- 2 years for non tinned chip capacitors,
- 3 years for gold plated chip capacitors.

STORAGE IN CONTROLLED NEUTRAL NITROGEN ENVIRONMENT:

- 4 years for tin dipped or electroplated chip capacitors,
- 4 years for non tinned chip capacitors,
- 5 years for gold plated chip capacitors.

Storage duration should be considered from delivery date and not from batch manufacture date. The tests carried out at final acceptance stage (solderability, susceptibility to solder heat) enable to assess the compatibility to surface mounting of the chips.

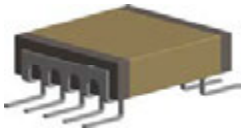
LEAD STYLES

SURFACE MOUNTING

DIL LEADS

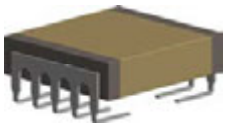
P style

PL style



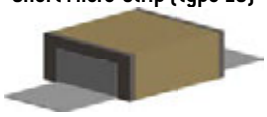
L style

J style

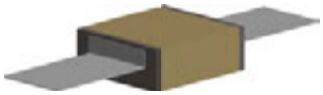


RIBBON LEADS

Micro-strip (type 1)
Short Micro-strip (type 1S)

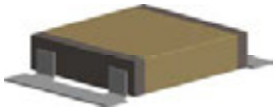


Axial (Type 2)

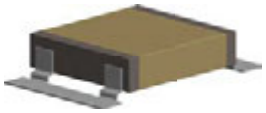


Radial (Type 3)

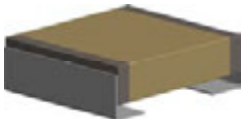
R style



RX style



RJ style



Please contact Exxelia sales for any lead configuration not shown.

TROUGH-HOLE MOUNTING

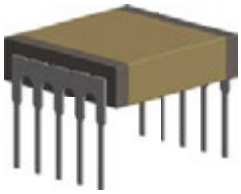
AXIAL AND RADIAL

Radial leads (Type 6)

Radial leads (4 leads)

Axial leads (Type 7)

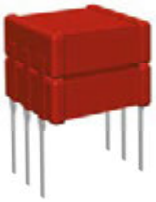
DIL leads: N style



ENCAPSULATION STYLES

Ceramic encapsulation
(selfprotected)

Varnish

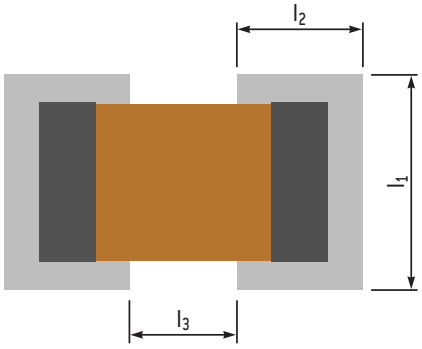


Conformal coating

Molding

User Guide

SOLDERING ADVICES FOR REFLOW SOLDERING



Large chips above size 2225 are not recommended to be mounted on epoxy board due to thermal expansion coefficient mismatch between ceramic capacitor and epoxy. Where larger sizes are required, it is recommended to use components with ribbon or other adapted leads so as to absorb thermo-mechanical strains.

Dimensions in inches (in mm)	Reflow soldering						Wave soldering					
	I_1		I_2		I_3		I_1		I_2		I_3	
0402	0.043	(1.1)	0.035	(0.9)	0.012	(0.3)	0.043	(1.1)	0.047	(1.2)	0.012	(0.3)
0403	0.055	(1.4)	0.035	(0.9)	0.012	(0.3)	0.055	(1.4)	0.047	(1.2)	0.012	(0.3)
0504	0.063	(1.6)	0.051	(1.3)	0.016	(0.4)	0.063	(1.6)	0.063	(1.6)	0.016	(0.4)
0603	0.055	(1.4)	0.059	(1.5)	0.02	(0.5)	0.055	(1.4)	0.071	(1.8)	0.02	(0.5)
0805	0.073	(1.85)	0.065	(1.65)	0.024	(0.6)	0.073	(1.85)	0.077	(1.95)	0.024	(0.6)
0907	0.094	(2.4)	0.065	(1.65)	0.035	(0.9)	0.094	(2.4)	0.077	(1.95)	0.035	(0.9)
1005	0.073	(1.85)	0.067	(1.7)	0.039	(1)	0.073	(1.85)	0.079	(2)	0.039	(1)
1206	0.083	(2.1)	0.067	(1.7)	0.059	(1.5)	0.083	(2.1)	0.079	(2)	0.059	(1.5)
1210	0.118	(3)	0.069	(1.75)	0.059	(1.5)	0.118	(3)	0.081	(2.05)	0.059	(1.5)
1605	0.073	(1.85)	0.071	(1.8)	0.087	(2.2)	0.073	(1.85)	0.083	(2.1)	0.087	(2.2)
1806	0.087	(2.2)	0.073	(1.85)	0.102	(2.6)	0.087	(2.2)	0.085	(2.15)	0.102	(2.6)
1812	0.152	(3.85)	0.073	(1.85)	0.102	(2.6)	0.152	(3.85)	0.085	(2.15)	0.102	(2.6)
1825	0.281	(7.15)	0.073	(1.85)	0.102	(2.6)	0.281	(7.15)	0.085	(2.15)	0.102	(2.6)
2210	0.13	(3.3)	0.079	(2)	0.146	(3.7)	0.13	(3.3)	0.091	(2.3)	0.146	(3.7)
2220	0.228	(5.8)	0.079	(2)	0.146	(3.7)	0.228	(5.8)	0.091	(2.3)	0.146	(3.7)
2225	0.281	(7.15)	0.079	(2)	0.146	(3.7)	0.281	(7.15)	0.091	(2.3)	0.146	(3.7)

RECOMMENDED FOOTPRINT FOR SMD CAPACITORS

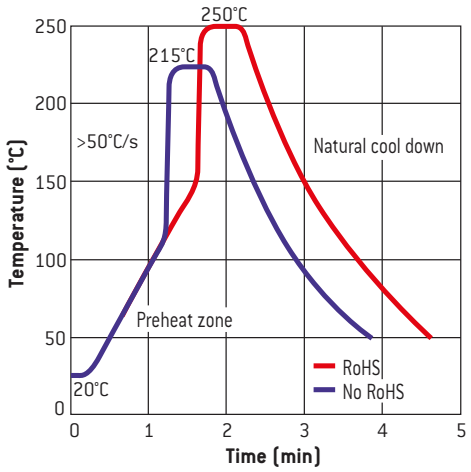
Ceramic is by nature a material which is sensitive both thermally and mechanically. Stresses caused by the physical and thermal properties of the capacitors, substrates and solders are attenuated by the leads.

Wave soldering is unsuitable for sizes larger than 2220 and for the higher ends of capacitance ranges due to possible thermal shock (capacitance values given upon request).

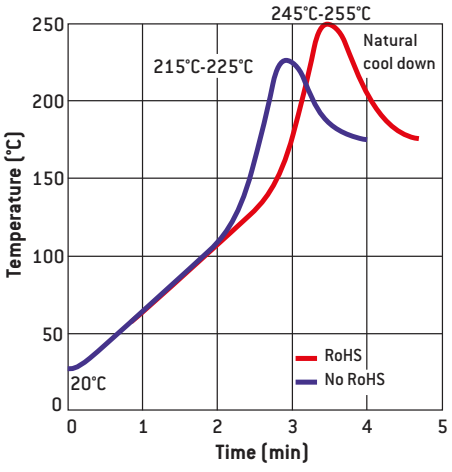
Infrared and vapor phase reflow, are preferred for high reliability applications as inherent thermo-mechanical strains are lower than those inherent to wave soldering.

Whatever the soldering process is, it is highly recommended to apply a thermal cycle, see hereafter our recommended soldering profile:

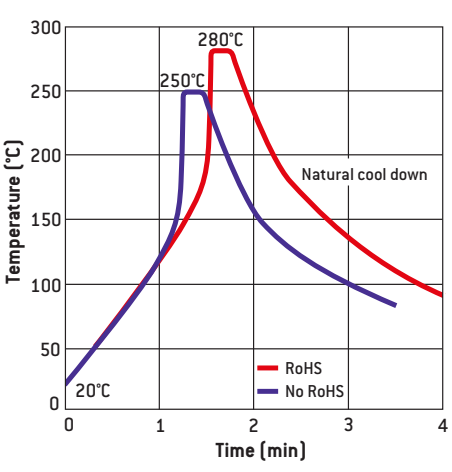
RECOMMENDED VAPOR PHASE REFLOW PROFILE



RECOMMENDED IR REFLOW PROFIL



RECOMMENDED WAVE SOLDERING PROFILE



SOLDERING ADVICES FOR IRON SOLDERING

Attachment with a soldering iron is discouraged due to ceramic brittleness and the process control limitations. In the event that a soldering iron must be used, the following precautions should be observed:

- Use a substrate with chip footprints big enough to allow putting side by side one end of the capacitor and the iron tip without any contact between this tip and the component,
- place the capacitor on this footprint,
- heat the substrate until the capacitor's temperature reaches 150° C minimum (preheating step, maximum 1°C per second),
- place the hot iron tip (a flat tip is preferred) on the footprint **without touching the capacitor.** Use a regulated iron with a 30 watts maximum power. The recommended temperature of the iron is 270 ±10° C. The temperature gap between the capacitor and the iron tip must not exceed 120° C,
- leave the tip on the footprint for a few seconds in order to increase locally the footprint's temperature,
- use a cored wire solder and put it down on the iron tip. In a preferred way use Sn/Pb/Ag 62/36/2 alloy,
- wait until the solder fillet is formed on the capacitor's termination,
- take away iron and wire solder,
- wait a few minutes so that the substrate and capacitor come back down to the preheating temperature,
- solder the second termination using the same procedure as the first,
- let the soldered component cool down slowly to avoid any thermal shock.

PACKAGING

TAPE AND REEL

The films used on the reels correspond to standard IEC 60286-3. Films are delivered on reels in compliance with document IEC 286-3 dated 1991.

Minimum quantity is 250 chips.

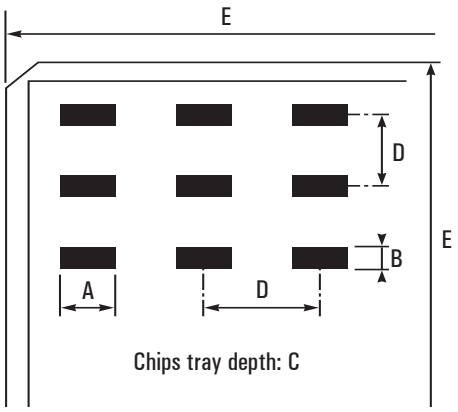
Maximum quantities per reel are as follows:

- Super 8 reel - Ø 180: 2,500 chips.
- Super 8 reel - Ø 330: 10,000 chips.
- Super 12 reel - Ø 180: 1,000 chips.

Reel marking complies with CECC 32100 standard:

- Model.
- Rated capacitance.
- Capacitance tolerance.
- Rated voltage.
- Batch number.

TRAY PACKAGES



DIMENSIONAL CHARACTERISTICS OF CHIPS TRAY PACKAGES

Sizes	Nr. of chips/ package	Oriented chips	Dimensions in inches (in mm)				
			A	B	C	D	E
0402	100	No	Ø 0.112 (Ø 3.02)		0.065 (1.65)	0.167 (4.24)	2 (50.8)
0403	100	No	Ø 0.112 (Ø 3.02)		0.065 (1.65)	0.167 (4.24)	2 (50.8)
0504	100	Yes	0.059 (1.5)	0.045 (1.14)	0.035 (0.89)	0.167 (4.24)	2 (50.8)
0603	340	Yes	0.1 (2.54)	0.06 (1.52)	0.045 (1.14)	0.167 (4.24)	2 (50.8)
0805	100	Yes	0.1 (2.54)	0.06 (1.52)	0.045 (1.14)	0.167 (4.24)	2 (50.8)
1206	100	No	0.14 (3.56)	0.14 (3.56)	0.06 (1.52)	0.167 (4.24)	2 (50.8)
1210	100	Yes	0.14 (3.56)	0.14 (3.56)	0.06 (1.52)	0.167 (4.24)	2 (50.8)
1812	100	No	0.25 (6.35)	0.25 (6.35)	0.13 (3.3)	0.345 (8.76)	4 (101.6)
	25	Yes	0.24 (6.1)	0.265 (6.73)	0.07 (1.78)	0.345 (8.76)	2 (50.8)
2220	100	Yes	0.25 (6.35)	0.25 (6.35)	0.13 (3.3)	0.345 (8.76)	4 (101.6)
	25	Yes	0.24 (6.1)	0.265 (6.73)	0.07 (1.78)	0.345 (8.76)	2 (50.8)

User Guide

EIA STANDARD CAPACITANCE VALUES

Following EIA standard, the values and multiples that are indicated in the chart below can be ordered. E48, E96 series and intermediary values are available upon request.

E6 (± 20%)	E12 (± 10%)	E24 (± 5%)
10	10	10
		11
	12	12
		13
15	15	15
		16
	18	18
		20
22	22	22
		24
	27	27
		30
33	33	33
		36
	39	39
		43
47	47	47
		51
	56	56
		62
68	68	68
		75
	82	82
		91

PART MARKING VOLTAGE CODES

Use the following voltage code chart for part markings:

Voltage (V)	Code	Letter code
25	250	A
40	400	B
50	500	C
63	630	D
100	101	E
200	201	G
250	251	H
400	401	K
500	501	L
1,000	102	M
2,000	202	P
3,000	302	R
4,000	402	S
5,000	502	T
7,500	752	U
10,000	103	W

EIA CAPACITANCE CODE

The capacitance is expressed in three digit codes and in units of pico Farads (pF). The first and second digits are significant figures of the capacitance value and the third digit identifies the multiplier.

For capacitance value < 10pF, R designates a decimal point.
See examples below:

EIA code	Capacitance value		
	in pF	in nF	in µF
2R2	2.2	0.0022	0.0000022
6R8	6.8	0.0068	0.0000068
220	22	0.022	0.000022
470	47	0.047	0.000047
181	180	0.18	0.00018
221	220	0.22	0.00022
102	1,000	1	0.001
272	2,700	2.7	0.0027
123	12,000	12	0.012
683	68,000	68	0.068
124	120,000	120	0.12
564	560,000	560	0.56
335	3,300,000	3,300	3.3
825	8,200,000	8,200	8.2
156	15,000,000	15,000	15
686	68,000,000	68,000	68
107	100,000,000	100,000	100
227	220,000,000	220,000	220

PART MARKING TOLERANCE CODES

Use the following tolerance code chart for part markings:

Tolerance	Letter code
±0.25pF	CU
±0.5pF	DU
±1pF	FU
±1%	F
±2%	G
±5%	J
±10%	K
±20%	M

RELIABILITY LEVELS

Exxelia proposes different reliability levels for the ceramic capacitors for both NP0 and X7R ceramics.