

MIL-STD 1553 Interface Transformers - DBIT x 5 S(A)



- In accordance to MIL-STD 1553 A&B
- Meet all the electrical requirements of Manchester II serial bi-phase data transmission, 1 MHz operation
- Epoxy molding in accordance with outgassing requirements of ECSS-Q-ST-70-02C
- Qualified EPPL
- Open-circuit impedance greater than 4 kΩ over 75 KHz to 1 MHz working frequency
- Frequency range 75 KHz to 1 MHz
- Operating temperature range: -55°C up to +150°C
- Weight: 3 to 3.5 grams

Electrical Data (25°C)

ID Code	Turn ratio 1-3 : 4-8	Turn ratio 1-3 : 5-7	DCR max. (Ω) 1-3	DCR max. (Ω) 4-8	Primary Inductance (mH) min at 75 kHz-1V	Open Circuit Impedance Min (kΩ)	Operating temperature range
DBIT 1 5S*	1,4:1	2:1	2,2	1,2	7 (1-3)	3	-55°C +125°C
DBIT 2 5S*	1:1	1:0,707	2,2	2,4	7 (1-3)	3	-55°C +125°C
DBIT 3 5S*	1,2:1	1,67:1	2,2	2	7 (1-3)	3	-55°C +125°C
DBIT 4 5S*	1:2,5	1:1,74	1,2	2,7	7 (4-8)	3	-55°C +125°C
DBIT 5 5S*	1:2,5	1:1,79	1,2	2,7	7 (4-8)	3	-55°C +125°C
DBIT 6 5S*	2,3:1	3,2:1	2,2	1,2	7 (1-3)	3	-55°C +125°C
DBIT 7 5S*	1,25:1	1,66:1	2,2	2	7 (1-3)	3	-55°C +125°C
DBIT 8 5S*	1:2,12	1:1,5	1,2	2,7	7 (4-8)	3	-55°C +125°C
DBIT 1 5SA	1,4:1	2:1	1,23	1,1	7 (1-3)	4	-55°C +150°C
DBIT 2 5SA	1:1	1:0,707	1,23	1,6	7 (1-3)	4	-55°C +150°C
DBIT 3 5SA	1,2:1	1,67:1	1,23	1,4	7 (1-3)	4	-55°C +150°C
DBIT 5 5SA	1:2,5	1:1,79	0,6	1,4	7 (4-8)	4	-55°C +150°C
DBIT 6 5SA	2,3:1	3,2:1	1,23	0,8	7 (1-3)	4	-55°C +150°C
DBIT 7 5SA	1,25:1	1,66:1	1,23	1,25	7 (1-3)	4	-55°C +150°C
DBIT 8 5SA	1:2,12	1:1,5	0,7	1,4	7 (4-8)	4	-55°C +150°C

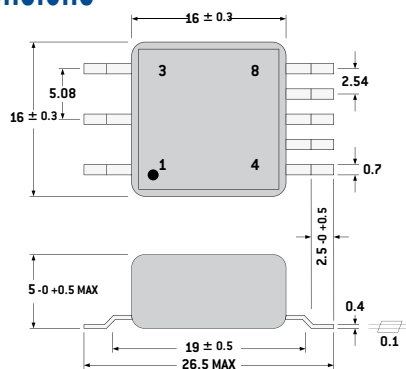
* EPPL products - Detail Specifications MSP003

To Order

DBIT	#	5	S	A
Range	Part 1 to 8	Case height 5	S SMD	New version

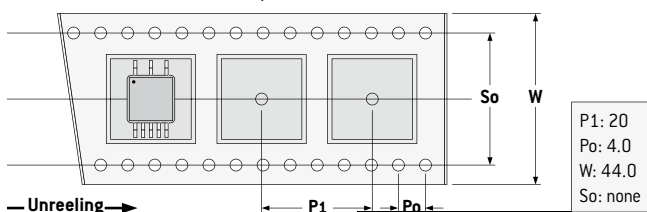
DBIT # 5SA

Typical Dimensions (mm, top view)



Packaging

Individually packed: 32 parts on 2 layers.
Tape and Reel:
200 units per reel of diameter 330 mm

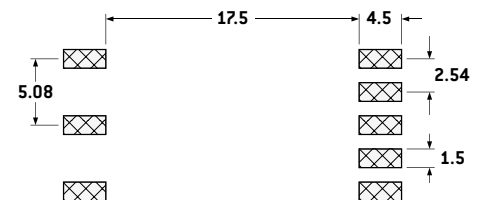


P1: 20
Po: 4.0
W: 44.0
So: none

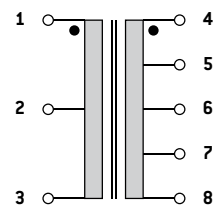
Notes

- Common mode rejection : 45 dBmin.
- Dielectric withstanding voltage : 500Vrms.
- Insulation resistance : 1,3 - 4,8 500 V_{DC} >1000 MΩ
- tolerance ratio ± 3%.

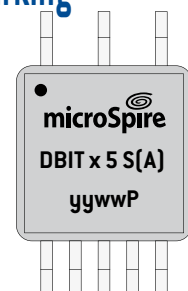
PCB Layout (suggested)



Connections



Marking



yyww :
Date code